IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device having active regions connected together by interconnect layers comprising:

~~a semiconductor substrate;~~

first and second transistors formed spaced apart from each other in a semiconductor substrate, each of the first and second transistors having active regions ~~each having a gate electrode and a pair of active regions, the pair of active regions being formed in the semiconductor substrate~~;

an isolation region formed :between the first and second transistors in the semiconductor substrate for isolating the first and second transistors from each other;

at least one slit formed in ~~a top surface region~~ the surface of the isolation region to allow those paired active regions of the first and second transistors which are opposed to each other with the isolation region interposed therebetween to communicate with each other through it, the slit having inner walls and a predetermined width;

a conductive layer formed on the inner walls of the slit; and

an interconnect layer having first and second portions respectively formed on the paired active regions of the first and second transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region, the first, second and third portions being made integral with one another, ~~and the interconnect layer having a top surface which is lower than a top surface of the gate electrode~~

wherein the interconnect layer has a stacked structure including a lower layer of silicon and an upper layer of metal silicide.

Claim 2 (Original): The device according to claim 1, wherein the at least one slit consists of one slit.

Claim 3 (Original): The device according to claim 1, wherein the at least one slit consists of a plurality of slits parallel with one another.

Claim 4 (Original): The device according to claim 1, wherein the slit has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit can be substantially filled up with the third portion of the interconnect layer.

Claim 5 (Original): The device according to claim 4, wherein the minimum value of the slit width is 0.03 μm and the maximum value is 0.1 μm.

Claim 6 (Original): The device according to claim 1, wherein a depth of the slit is less than that of the isolation region.

Claim 7 (Original): The device according to claim 1, wherein the conductive layer is a silicon-containing film.

Claim 8 (Original): The device according to claim 7, wherein the silicon-containing film is a polysilicon film.

Claims 9-10 (Canceled).

Claim 11 (Original): The device according to claim 1, further comprising a contact portion formed on the third portion of the interconnect layer.

Claim 12 (Currently Amended): A semiconductor device having active regions connected together by an interconnect layer comprising:

~~a semiconductor substrate;~~

first and second MOS transistors formed spaced apart from each other in a semiconductor substrate, each of the first and second MOS transistors having a gate electrode and active regions ~~each having a gate electrode and a pair of active regions, the pair of active regions being formed in the semiconductor substrate~~;

an isolation region formed between the first and second MOS transistors in the semiconductor substrate for isolating the first and second MOS transistors from each other;

at least one slit formed in ~~a top surface region~~ the surface of the isolation region to allow paired active regions of the first and second MOS transistors, which are opposed to each other with the isolation region interposed therebetween, to communicate with each other through it, the slit having inner walls and a predetermined width;

a conductive layer formed on the inner walls of the slit;

a gate electrode of another MOS transistor formed above the isolation region; and

an interconnect layer having first and second portions respectively formed on the paired active regions of the first and second MOS transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region to ride on and be electrically connected with the gate electrode of another transistor, the first, second and third portions being made

integral with one another, ~~and the interconnect layer having a top surface which is lower than a top surface of the gate electrode~~

wherein the interconnect layer has a stacked structure including a lower layer of silicon and an upper layer of metal silicide.

Claim 13 (Original): The device according to claim 12, wherein the at least one slit consists of one slit.

Claim 14 (Original): The device according to claim 12, wherein the at least one slit consists of a plurality of slits parallel with one another.

Claim 15 (Original): The device according to claim 12, wherein the slit has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit can be substantially filled up with the third portion of the interconnect layer.

Claim 16 (Original): The device according to claim 15, wherein the minimum value of the slit width is 0.03 μm and the maximum value is 0.1 μm.

Claim 17 (Original): The device according to claim 12, wherein a depth of the slit is less than that of the isolation region.

Claim 18 (Original): The device according to claim 12, wherein the conductive film is a silicon-containing film.

Claim 19 (Original): The device according to claim 18, wherein the silicon-containing film is a polysilicon film.

Claims 20-21 (Canceled).

Claim 22 (Original): The device according to claim 12, further comprising a contact portion formed on the third portion of the interconnect layer.

Claims 23-44 (Canceled).

Claim 45 (New): A semiconductor device having active regions connected together by interconnect layers comprising:

first and second transistors formed spaced apart from each other in a semiconductor substrate, each of the first and second transistors having active regions;

an isolation region formed between the first and second transistors in the semiconductor substrate for isolating the first and second transistors from each other;

at least one slit formed in the surface of the isolation region to allow those paired active regions of the first and second transistors which are opposed to each other with the isolation region interposed therebetween to communicate with each other through it, the slit having inner walls and a predetermined width;

a conductive layer formed on the inner walls of the slit; and

an interconnect layer having first and second portions respectively formed on the paired active regions of the first and second transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed

along the slit on the isolation region, the first, second and third portions being made integral with one another,

wherein the interconnect layer has a stacked structure including a lower layer of an alloy of silicon and germanium and an upper layer of silicide of an alloy of silicon and germanium.

Claim 46 (New): The device according to claim 45, wherein the at least one slit consists of one slit.

Claim 47 (New): The device according to claim 45, wherein the at least one slit consists of a plurality of slits parallel with one another.

Claim 48 (New): The device according to claim 45, wherein the slit has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit can be substantially filled up with the third portion of the interconnect layer.

Claim 49 (New): The device according to claim 48, wherein the minimum value of the slit width is 0.03 μm and the maximum value is 0.1 μm.

Claim 50 (New): The device according to claim 45, wherein a depth of the slit is less than that of the isolation region.

Claim 51 (New): The device according to claim 45, wherein the conductive layer is a silicon-containing film.

Claim 52 (New): The device according to claim 51, wherein the silicon-containing film is a polysilicon film.

Claim 53 (New): The device according to claim 49, further comprising a contact portion formed on the third portion of the interconnect layer.

Claim 54 (New): A semiconductor device having active regions connected together by an interconnect layer comprising:

first and second MOS transistors formed spaced apart from each other in a semiconductor substrate, each of the first and second MOS transistors having a gate electrode and active regions;

an isolation region formed between the first and second MOS transistors in the semiconductor substrate for isolating the first and second MOS transistors from each other;

at least one slit formed in the surface of the isolation region to allow paired active regions of the first and second MOS transistors, which are opposed to each other with the isolation region interposed therebetween, to communicate with each other through it, the slit having inner walls and a predetermined width;

a conductive layer formed on the inner walls of the slit;

a gate electrode of another MOS transistor formed above the isolation region; and

an interconnect layer having first and second portions respectively formed on the paired active regions of the first and second MOS transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region to ride on and be electrically connected

with the gate electrode of another transistor, the first, second and third portions being made integral with one another,

wherein the interconnect layer has a stacked structure including a lower layer of an alloy of silicon and germanium and an upper layer of silicide of an alloy of silicon and germanium.

Claim 55 (New): The device according to claim 54, wherein the at least one slit consists of one slit.

Claim 56 (New): The device according to claim 54, wherein the at least one slit consists of a plurality of slits parallel with one another.

Claim 57 (New): The device according to claim 54, wherein the slit has a minimum value of its width set to the minimum dimension determined by processing accuracy and a maximum value set such that the slit can be substantially filled up with the third portion of the interconnect layer.

Claim 58 (New): The device according to claim 57, wherein the minimum value of the slit width is 0.03 μm and the maximum value is 0.1 μm.

Claim 59 (New): The device according to claim 54, wherein a depth of the slit is less than that of the isolation region.

Claim 60 (New): The device according to claim 54, wherein the conductive film is a silicon-containing film.

Claim 61 (New): The device according to claim 60, wherein the silicon-containing film is a polysilicon film.

Claim 62 (New): The device according to claim 54, further comprising a contact portion formed on the third portion of the interconnect layer.